IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

App. No.	:	10/627,165	Confirmation No.: 2527
Applicant	:	Thomas Laursen et al.	
Filed	:	July 24, 2003	
Art Unit	:	1742	
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David K. Benson

DECLARATION UNDER 37 C.F.R. § 1.132

Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

I, Vishwas V. Hardikar, declare as follows:

1. I am a co-inventor of the subject matter claimed in patent application 10/627,165 entitled *Method for Planarizing a Work Piece* and filed July 24, 2003 ("the instant application"). My co-inventor is Thomas Laursen.

2. In May of 2000, I received a Doctor of Philosophy (PhD) in chemistry from Clarkson University located in Postdam, New York. In May of 1996, I received a Masters in chemistry from University of Pune located in Pune, India. In May of 1994, I received a Bachelor of Science (BS) from Bombay University located in Bombay, India.

3. Since June of 2000, my professional career has been in the field of semiconductor fabrication, including chemical mechanical planarization systems and techniques. I have been employed as an engineer by Novellus Systems, Inc., since June of 2002. Prior to my employment with Novellus, I was employed by Ferro Corporation, Inc., and NuTool, Inc. located in New York and California, respectively. In total, I have been employed in a professional capacity in the field of semiconductor fabrication for approximately seven years.

4. I have reviewed and understand United States Patent No. 6,245,676 entitled *Method of Electroplating Copper Interconnects* issued June 12, 2001 (Patent '676).

5. At the time of the invention claimed in the instant application, electroplating techniques conventionally employed in the semiconductor industry produced a relatively thick overburden (i.e., having a thickness well beyond 300 nanometers) including a substantially non-planar upper surface (i.e., having a step height well beyond 100 nanometers).

6. Soft polishing pads generally conform to a non-planar upper surface and, thus, remove material at a substantially constant rate across the upper surface. Soft polishing pads were consequently considered generally inadequate for planarizing a workpiece having an overburden including a substantially non-planar upper surface of the type produced by conventional electroplating techniques.

7. In contrast to soft polishing pads, hard polishing pads do not generally conform to a non-planar upper surface and, thus, remove material at different rates across the upper surface to thereby smooth out topographical irregularities. For at least this reason, it was conventional practice in the semiconductor industry at the time of the invention to utilize at least one hard polishing pad to planarize an electroplated workpiece.

8. As do the conventional electroplating techniques described above, the electroplating method utilized to form copper plated layer 37a shown and described in Patent '676 likewise yields a non-planar upper surface having a step height well beyond 100 nanometers.

9. I hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Subject Application or any patent which issues thereon.

Vishwas V. Hardikar

Dated: 05/29/2007